

AMENDMENTS TO THE CLAIMS

1. (Currently amended) A word length reduction circuit for quantizing an N-bit input signal sample into an n-bit output signal sample; the circuit comprising:

an input for receiving the N-bit input signal samples;

a quantizer coupled to the input, and arranged to output an n-bit signal corresponding to the N-bit input sample signal; and

an outer feedback loop comprising a loop filter, coupled between the output of the least significant N-n bits of the signal input to the quantizer being coupled to the loop filter, the output of the loop filter being provided to a subtractor the quantizer and subtraction means coupled to the word length reduction circuit input for subtracting a feedback signal from the input signal, the output of the loop filter being coupled to having an inner feedback loop coupled between the output and the input of the loop filter to form an inner feedback loop.

2. (Original) A circuit according to claim 1 wherein the loop filter comprises an integrator structure.

3. (Original) A circuit according to claim 1 wherein the loop filter is a sigma-delta loop filter.

4. (Canceled)

5. (Currently amended) A circuit according to claim 1 wherein the subtractor ~~means for subtracting~~ is an adder for coupling the outer feedback loop to the circuit input.

6. (Previously Presented) A circuit according to claim 5 further comprising a second adder for coupling the outer feedback loop to the input of the loop filter, such that the inner feedback loop signal is subtracted from the feed-back signal from the quantizer.

7. (Original) A circuit according to claim 1 wherein the loop filter coefficients are implemented using shifters.

8. (Previously Presented) A circuit according to claim 1, the loop filter further comprising limiters to limit signal levels and scaling factors to normalize signal dynamic ranges.

9. (Previously Presented) A Converter for converting a pulse coded modulation (PCM) digital audio signal to a pulse width modulated (PWM) digital audio signal for amplification in a digital amplifier; the Converter comprising:

a word length reduction circuit according to claim 1;

a modulator for converting the PCM signals to PWM signals, the modulator coupled to the output of the quantizing circuit.

10. (Previously Presented) A Converter according to claim 9 further comprising a Linearizer for receiving input signal samples and an output coupled to the input of the word length reduction circuit for providing linearized signal samples.

11. (Currently amended) A Converter according to claim 10 wherein the Linearizer comprises:

means for determining an intermediate sample between two adjacent input signal samples;

means for determining the polarity of the intermediate sample;

means for determining at what signal amplitude an input signal waveform defined by said input samples and the intermediate sample crosses a reference waveform by applying one of two estimation algorithms dependent on the polarity of the intermediate sample; and

means for outputting a linearized signal sample having an amplitude corresponding to the determined crossing amplitude.

12. (Original) A Converter according to claim 11 wherein the intermediate sample determining means is an interpolator.

13. (Original) A Converter according to claim 12 wherein the interpolator is a filter with a zero interleaved input.

14. (Original) A Converter according to claim 11 wherein the estimation algorithms are linear or straight line approximations.

15. (Original) A Converter according to claim 14 wherein the means for determining an intermediate sample and the means for determining the signal amplitude are merged by implementing the estimation algorithms:

$$y = \begin{cases} b(1 + c(1 + c)) & \text{if } b \geq 0 \\ b(1 + a(1 + a)) & \text{otherwise} \end{cases}$$

where:

$$a = \frac{w(n-1) - w(n-2)}{2}$$

$$b = w(n-1) - a/2$$

$$c = \frac{w(n) - w(n-2)}{4}$$

$w(n)$ = input signal sample at sample time n .

16. (Original) A Converter according to claim 11 wherein the signal amplitude determining means comprises implementing Taylor Series calculations.

17. (Original) A digital amplifier comprising a Word length Reduction circuit according to claim 1 or a Converter according to claim 9.

18. (Currently Amended) A word length reduction method for quantizing an N-bit input signal sample into an n-bit output signal sample; the method comprising:

receiving the N-bit input signal samples;

quantizing the input signal samples in order to output an n-bit signal corresponding to the N-bit input sample signal;

subtracting a feedback signal from the input signal, the feedback signal being derived from the least significant N-n bits of the signal to be quantized, from the output of the quantizer, and filtering the feedback signal with a loop filter having an inner feedback loop coupled between the output and the input of the loop filter.

19. (Original) A method according to claim 18 wherein the loop filter comprises an integrator structure.

20. (Original) A method according to claim 18 wherein the loop filter is a sigma-delta loop filter.

21. (Canceled)

22. (Original) A method for converting a pulse coded modulation (PCM) digital audio signal to a pulse width modulated (PWM) digital audio signal for amplification in a digital amplifier; the method comprising:

word length reducing an N-bit input signal sample into an n-bit output signal sample according to claim 18;

modulating said word length reduced PCM signals into PWM signals.

23. (Previously Presented) A method according to claim 22 further comprising linearizing said received input signal samples prior to said word length reduction.

24. (Previously Presented) A method according to claim 23 wherein the Linearizing comprises:

determining an intermediate sample between two adjacent input signal samples;

determining the polarity of the intermediate sample;

determining at what signal amplitude an input signal waveform defined by said input samples and the intermediate sample crosses a reference waveform by applying one of two estimation algorithms dependent on the polarity of the intermediate sample;

outputting a linearized signal sample having an amplitude corresponding to the determined crossing amplitude.

25. (Original) A method according to claim 24 wherein the intermediate sample determining comprises interpolation.

26. (Original) A method according to claim 24 wherein the estimation algorithms are linear or straight line approximations.

27. (Previously Presented) A method according to claim 26 wherein determining the intermediate sample and determining the signal amplitude are merged using the estimation algorithms:

$$y = \begin{cases} b(1 + c(1 + c)) & \text{if } b \geq 0 \\ b(1 + a(1 + a)) & \text{otherwise} \end{cases}$$

where:

$$a = \frac{w(n-1) - w(n-2)}{2}$$

$$b = w(n-1) - a/2$$

$$c = \frac{w(n) - w(n-2)}{4}$$

$w(n)$ = input signal sample at sample time n .

28. (Original) A method according to claim 24 wherein the signal amplitude determining comprises a Taylor Series calculation.

29. (Original) A method of digitally amplifying an audio signal comprising a Word length Reducing method according to claim 18 or a method of Converting according to claim 22.

30. (Original) A carrier medium carrying processor readable code for controlling a processor to carry out the method of claim 18.

31. (Currently amended) A noise shaper circuit for reducing the word length of a digital audio amplifier, the circuit comprising a quantizer in a feedback loop with a loop filter, the difference between the input and output of the quantizer being coupled to the input of the loop filter, wherein the circuit is arranged such that the input signal is unfiltered and the noise transfer function is $1/(1+G(z))$ where $G(z)$ is the loop filter.

32. (New) A word length reduction circuit for quantizing an N-bit input signal sample into an n-bit output signal sample, the circuit comprising:

an input for receiving the N-bit input signal samples;

a quantizer coupled to the input, and arranged to output an n-bit signal corresponding to the N-bit input sample signal;

an outer feedback loop comprising a loop filter coupled between the output of the quantizer and a subtractor coupled to the word length reduction circuit input for subtracting a feedback signal from the input signal, the loop filter having an inner feedback loop coupled between the output and the input of the loop filter and further comprising limiters to limit signal levels and scaling factors to normalize signal dynamic ranges.

33. (New) A Converter for converting a pulse coded modulation (PCM) digital audio signal to a pulse width modulate (PWM) digital audio signal for amplification in a digital amplifier; the Converter comprising:

a word length reduction circuit for quantizing an N-bit input signal sample into a n-bit output signal sample, the circuit comprising:

an input for receiving the N-bit input signal samples;

a quantizer coupled to the input, and arranged to output an n-bit signal corresponding to the N-bit input sample signal;

an outer feedback loop comprising a loop filter coupled between the output of the quantizers and a subtractor coupled to the word length reduction circuit input for subtracting a feedback signal from the input signal, the loop filter having an inner feedback loop coupled between the output and the input of the loop filter;

a modulator for converting the PCM signals to PWM signals, the modulator coupled to the output of the quantizing circuit; and

a Linearizer for receiving input signal samples and an output coupled to the input of the word length reduction circuit for providing linearized signal samples, the Linearizer comprising:

means for determining an intermediate sample between two adjacent input signal samples;

means for determining the polarity of the intermediate sample;

means for determining at what signal amplitude an input signal waveform defined by said input samples and the intermediate sample crosses a reference

waveform by applying one of two estimation algorithms dependent on the polarity of the intermediate sample; and

means for outputting a linearized single sample having an amplitude corresponding to the determined crossing amplitude.

34. (New) A method for converting a pulse coded modulation (PCM) digital audio signal to a pulse width modulated (PWM) digital audio signal for amplification in a digital amplifier; the method comprising:

word length reducing an N-bit input signal sample into an n-bit signal by:

receiving the N-bit input signal samples;

quantizing the input signal samples in order to output an n-bit signal corresponding to the N-bit input sample signal;

subtracting a feedback signal from the input signal, the feedback signal derived from the output of the quantizer, and filtering the feedback signal with a loop filter having an inner feedback loop coupled between the output and the input of the loop filter; and

modulating said word length reduced PCM signals into PWM signals, linearizing said received input single samples prior to said word length reduction, wherein the Linearizing comprises:

determining an intermediate sample between two adjacent input signal samples;

determining the polarity of the intermediate sample;

determining at what signal amplitude an input signal waveform defined by said input samples and the intermediate sample crosses a reference waveform by applying one or two estimation algorithms dependent on the polarity of the intermediate sample;

outputting a linearized signal sample having an amplitude corresponding to the determined crossing amplitude.